Data Sheet

BI3101A

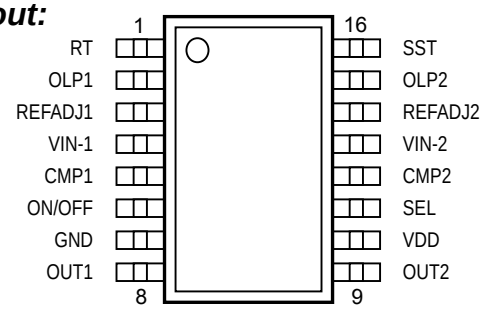
Dual PWM CCFL Controller

Version : 1.4

Features:

- **Dual PWM Modulators**
- **Dual Independent Open Lamp Protection**
- **On/Off control**
- **Flexible Dimming Scheme**
- **Internal UVLO (Under Voltage Look Out) function**
- **CMOS Totem Pole output**
- **NMOS output driving**
- **SOP Packing**

Pin Layout:



Applications:

- **Cold Cathode Fluorescent Lamps system**
- **LCD Monitor**
- **Notebook Computer**
- **LCD PC**
- **Palm-top Computers**
- **Video Phone/ Door Phone**
- **Portable Instrumentation**
- **Airline Entertainment Centers**
- **Automotive Display**
- **Personal Digital Assistants**
- **ATM/ Financial Terminal**
- **POS Terminal**
- **Test Equipment**
- **Navigation Devices (GPS Equipment)**
- **Copiers and Office Equipment**

General Description:

To aim at the Cold Cathode Fluorescent Lamp (CCFL) applications, the Bi3101A integrated all functions required in a single 16-pin chip. The chip provides 2 fully functioned PWM control circuit both with the true lamp current feedback. By setting the required time for striking the lamp through SST (Soft Start), the open-lamp condition can be detected after lamp striking period. ON/OFF control function will be very helpful for engineers to prevent the non-necessarily system power shut down. The lamp dimming can be done through this feedback loop or, by setting the reference DC level of the input of error amplifier. The reference DC level of dimming can be selected as higher level for more brightness or lower level for less brightness. CMOS process reduces the operating current and NMOS output driving capability enhances the system efficiency.

Patent pending.

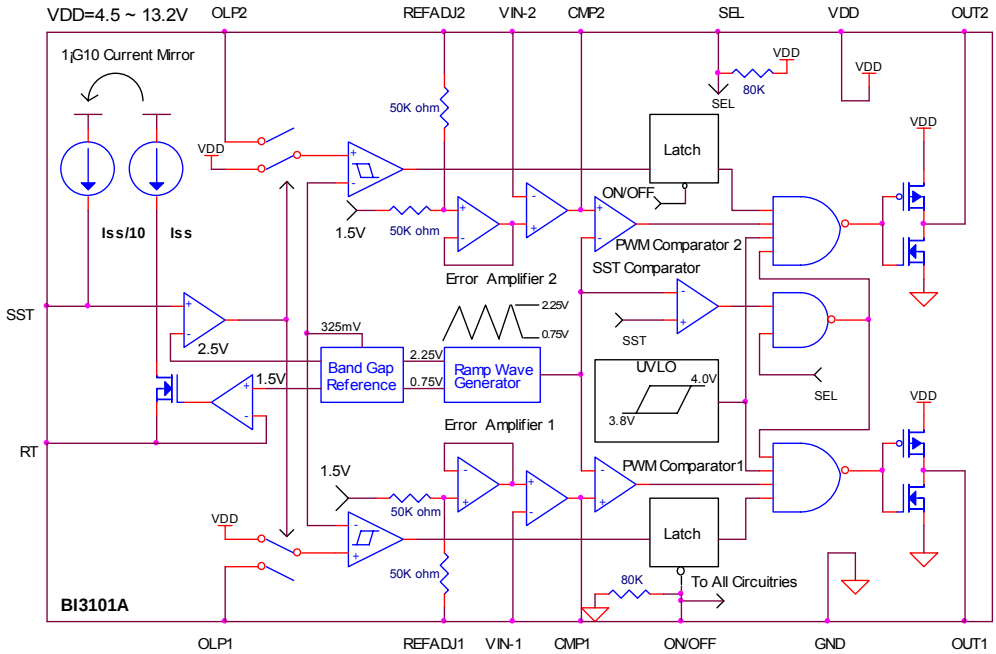
Absolute Ratings: *(if Ta=25℃)*

VDD……-0.3 ~+15 V
GND……±0.3 V
Input Voltage……-0.3 ~ VDD+0.3
Power Dissipation……40 mW
Operating Ambit Temperature……0 ~ +70 ℃
Operating Junction Temperature……+150 ℃
Storage Temperature……-55~+150 ℃

Recommended Operating Condition:

Supply Voltage……4.5 ~ 13.2 V
Operating Ambient Temperature……0 ~ 70 ℃
Operating Frequency……50K ~ 250K Hz

Functional Block Diagram:



Function Description:

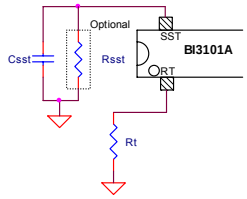
UVLO: The under-voltage-lookout circuit turns the output driver off when supplying voltage drops to a specified low level.

Band Gap Reference: This circuit provides a accuracy voltage source which is very stable even though the operating temperature is variable. To amplify or divide this reference can get the required voltage.

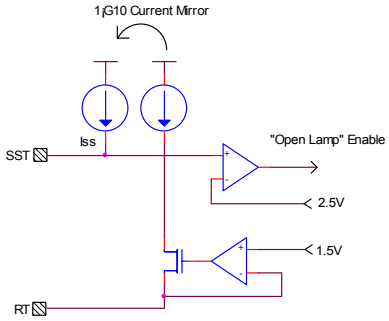
Ramp Wave Generator: This circuit generates a typically 140KHz ramp wave. (as Rt = 100 kΩ) Freq.(KHz)=14000/Rt(KΩ)

Open Lamp Protection: The current source Iss charges the external resistor and capacitor during power-on procedure. The voltage drops on the SST pin will be increased with Vsst =Iss x T;

Iss = 1.5V/(Rt x 10) where V_{RT} =1.5V



The protection circuit will be enabled when V_{SST} > 2.5V to prevent transformer working at extremely high voltage for a long time.



The required time for striking the lamp could be calculated as bellow:

$T_{STRIKE} = Vsst|_{2.5V} \div Iss = 16.67 \times Rt \times Csst$ (s)

The open lamp protection function is disabled when Vsst < 2.5V .

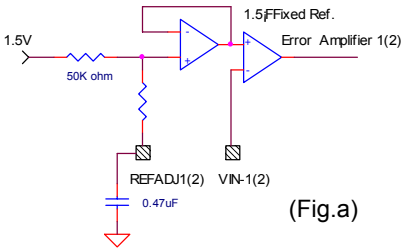
The latch-off situation can be removed by turning the power off or reset the On/Off control.

PWM Controller: The pulse width modulation control circuit includes a ramp wave generator, an error amplifier and a comparator. These devices provide the required active components for the PWM feedback control application.

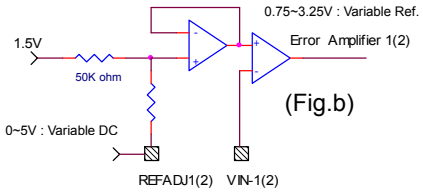
On/Off control: This pin can enable or disable the chip without turning off the power. Only approximately 40 nA leakage current consumption occurs when the chip is turned off. The chip will be woken up if a 2.5 V or higher input is applied on this pin and the soft-start procedure will conduct. This function can be used to restart the chip when open lamp is detected.

Dual Open Lamp Protection: If a voltage level which is less than 325mV is sensed from OLP1 or OLP2, indicates that this lamp is an open circuit, the related PWM circuit will be shut down and never restart until the power is turned off and on again or ON/OFF function is enabled. OLP1 and OLP2 work independently. Either one open lamp is detected and shut down but another PWM circuit will work normally. It can be used to shut down one of the PWM circuits for one lamp application.

REFADJ: The reference voltage of error amplifier can be decided as a fixed level or variable levels. If the REFADJ pin is connected to a 0.47uF capacitor then to the ground (means DC floating), the reference voltage of error amplifier will be 1.5 Vdc. This fixed reference voltage comparing to a variable VIN voltage than make a zero-volt-most-bright dimming system. (Fig.a)



(Fig.a)



(Fig.b)

If the REFADJ pin is connected to a DC level from 0V to 5V of 12V VDD operating, the reference voltage of error amplifier will be from 0.75V to 3.25V. This variable reference voltage comparing to a fixed VIN voltage than make a zero-volt-most-dark dimming system. (Fig.b)

Pin Description:

Pin No.	Names	Description
1	RT	Operation frequency control.
2	OLP1	A voltage sense input pin. If voltage level is less than 325 mV after a user defined period of time, the chip will shut down the OUT1 and PWM_1 citcuirs. A digital latch circuit latches this result. The latch condition will be released if the power be turned off and on again or disable the chip by setting the ON/OFF pin to off state.
3	REFADJ1	PWM_1 controller input, reference level adjustment pin of the error amplifier_1.
4	Vin-1	PWM_1 controller input, the inverting input of error amplifier_1.
5	CMP1	PWM_1 controller input, the output of error amplifier_1.
6	ON/OFF	Enable and disable Control. The chip only consumes the leakages current when it is disable.
7	GND	Ground.

Pin No.	Names	Description
8	OUT1	PWM_1 output, logic high active for driving NMOS device.
9	OUT2	PWM_2 output, logic active for driving NMOS device.
10	VDD	Supply voltage.
11	SEL	Soft -Start selection, a ground SEL makes Bi3101A works as the same as Bi3101. An internal pull-high resistor is integrated internally. A long period and programmable soft start control scheme is selected via floating SEL.
12	CMP2	PWM_2 controller input, the output of error amplifier_2.
13	Vin-2	PWM_2 controller input, the inverting input of error amplifier_2.
14	REFADJ2	PWM_2 controller input, reference level adjustment pin of the error amplifier_2.
15	OLP2	A voltage sense input pin. If voltage level is less than 325 mV after a user defined period of time, the chip will shut down the OUT2 and PWM_2 circuits. A digital latch circuit latches this result. The latch condition will be released if the power be turned off and on again or disable the chip by setting the ON/OFF pin to off state.
16	SST	The timer for soft start and open lamp protection.

DC/AC Characteristics:

Parameter	Test Conditions	Min.	Typ.(Limits)	Max.	Unit
Reference Voltage					
Output voltage	Measure Vin- VDD=12V. Ta=25°C	1.495	1.5	1.545	V
Line regulation	VDD=4.5 ~ 13.2 V		2	20	mV
Under Voltage Look Out					
Upper threshold voltage	Ta=25℃	3.8	4	4.2	V
Hysteresis		0.1	0.2	0.3	V
Ramp Wave Generator					
Frequency	Rt=100K Ω	120	140	160	KHz
Operating Frequency	note 1	50		250	KHz
Output peak			2.25		V
Output valley			0.75		V
Error Amplifier					
Input voltage	note 1	0.75		2.25	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
SST Soft Start and Open Lamp Enable					
Output current	VDD=12V, Ta=25℃		1.5V/Rt		uA
Open lamp detection enable			2.5		V
Open Lamp Protection					
Open lamp detection lower threshold	VDD=12V, Ta=25℃		325		mV
Hysteresis			50		mV
Output					
CMOS output impedance	note 1		50		Ω
Rising Time	1000pF load, note 1		110		ns
Falling Time			100		ns

Ta : ambient temperature.

Note 1: It is guaranteed by design not 100% tested.

Timing Diagrams:

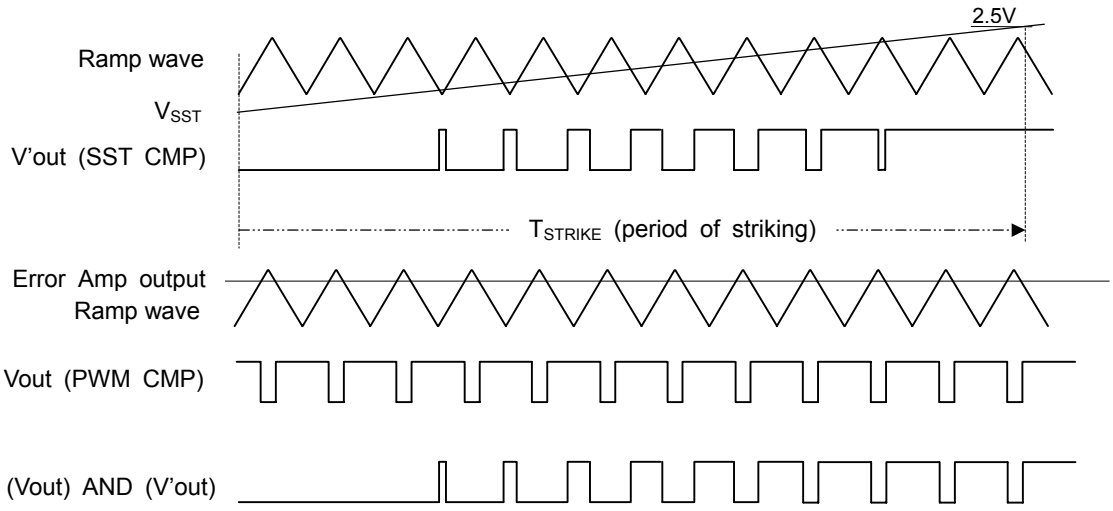
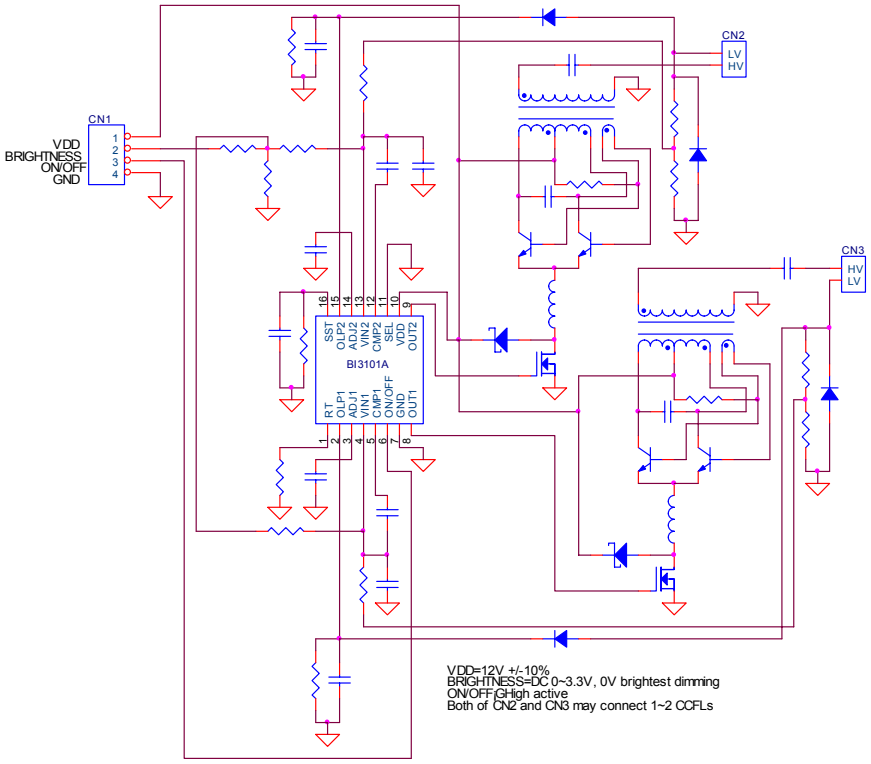


Fig. 1 The timing drawing of SEL floating soft start

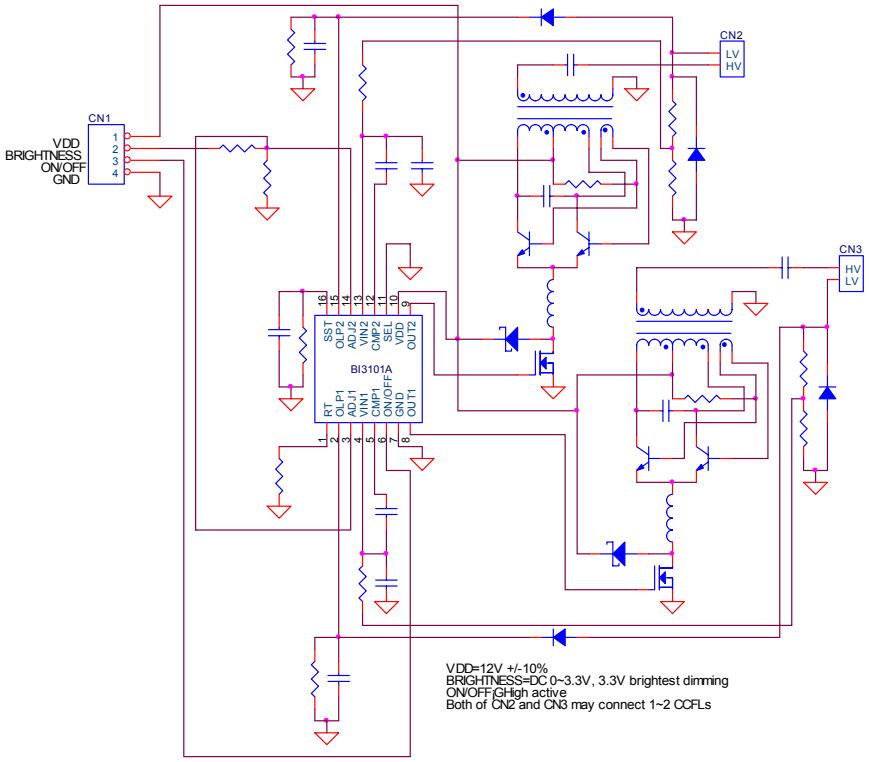
Bi3101A provides two configurations to start the CCFL by SEL pin. One is a grounded SEL pin that makes Bi3101A works just as the same as Bi3101. "Soft start" can be achieved by slowly increasing the reference voltage with the embedded R-C circuit. But for some applications, it may need a long period and programmable of "soft start" to prevent the inrush current during "Power On" sequence. Then a floating SEL pin enables the SST comparator of Bi3101A. With the two inputs of the SST voltage and the internal ramp-wave, the output is a "AND" logic of the output of SST comparator and the PWM comparator output. If a large capacitor of Csst is properly selected, a long and programmable "soft start period " is obtained. Please refer to the Function Block Diagram. Fig.1 is the timing diagram of floating SEL .

Application Information:

Bi3101A provides engineer more possibilities while facing diversity of electronic system design. Four examples are here.

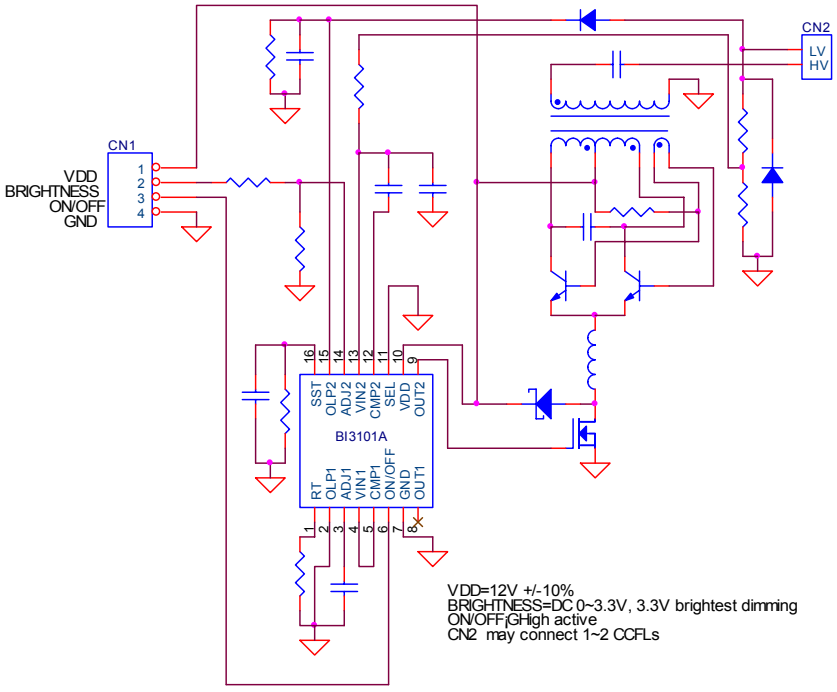


Example 1 :
This is a typical design for 2 to 4 lamps system. ON/OFF control can turn off the lamps without shout the VDD down.



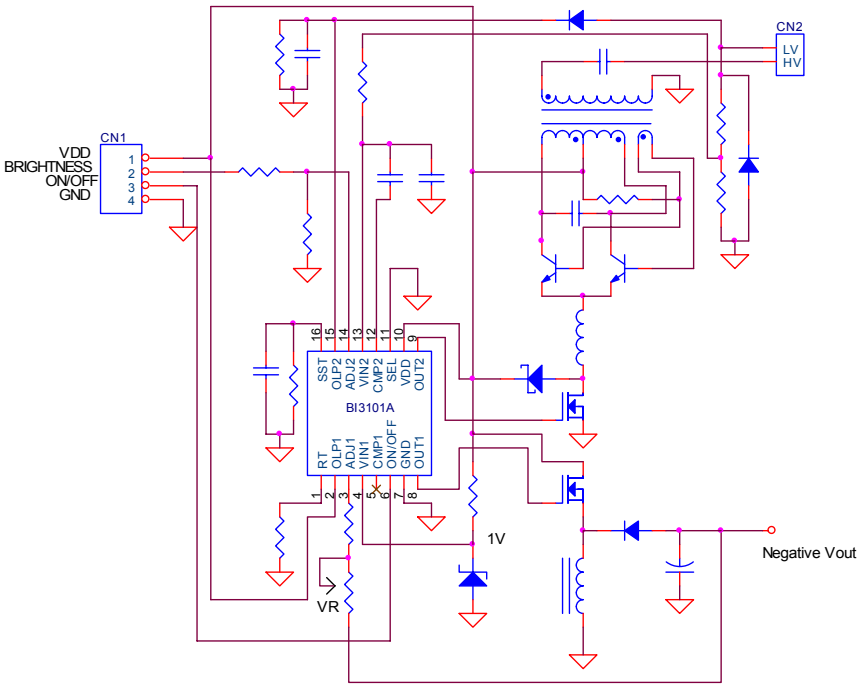
Example 2 :

This is a different dimming scheme from example 1, zero-volt-most-dark.



Example 3 :

The independent design of open lamp protection makes Bi3101A can used as a single PWM controller without consuming the extra power. A force-to-GND connection of OLP pin will shut down the circuit of PWM. This is an example of Bi3101A operates as a single PWM modulator.



VDD=12V +/-10%
BRIGHTNESS=DC 0~3.3V, 3.3V brightest dimming
ON/OFF¡GHigh active
CN2 may connect 1~2 CCFLs
Negative Vout could be used as LCD contrast bias

Example 4 :
When a negative voltage is required in LCD display systems, this example is used for both CCFL control and generating LCD negative bias.

Order Information:

Bi3101A-SO

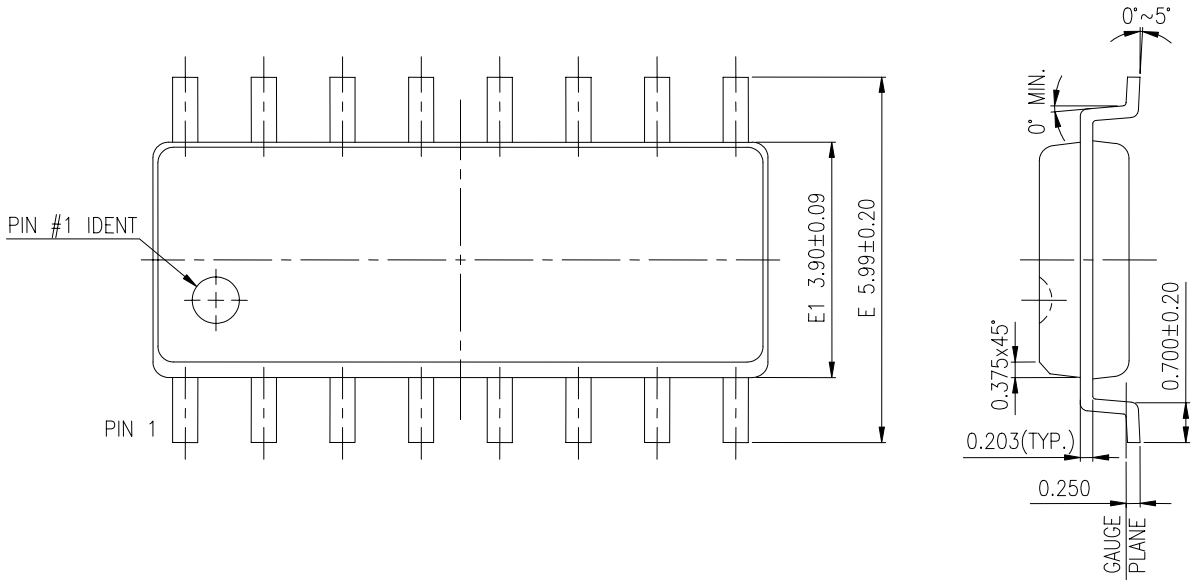
- **SOP** type packing
- Part number
- Beyond Innovation Technology Co., Ltd.

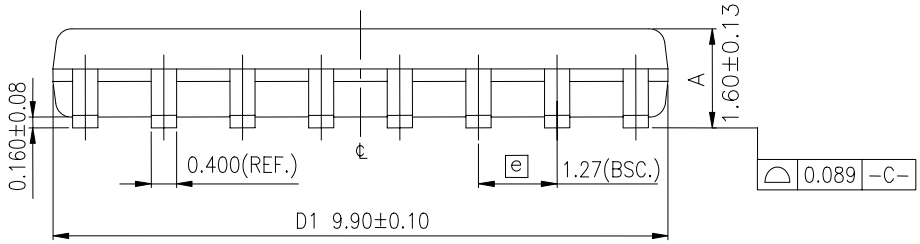
Bi3101A-DP

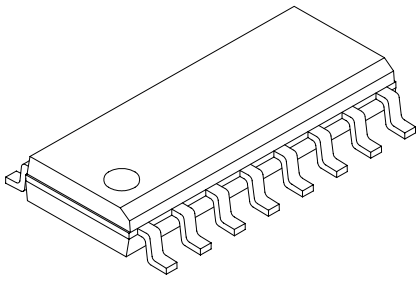
- **DIP** type packing
- Part number
- Beyond Innovation Technology Co., Ltd.

Package Information :

Unit: mm







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Unit: mm