



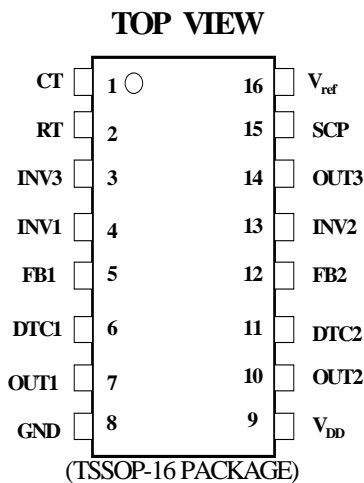
Preliminary and Provisional

BUCK_BOOST & BOOST PWM CONTROLLER WITH ADJUSTABLE LDO

Features

- Complete PWM Power Control Circuitry
CH-1: buck_boost, CH-2: boost
- Adjustable LDO Regulator
- Under-voltage Lockout Protection
- Totem pole Output
- Output Short Circuit Protection
- Dead Time Control : 0 to 100%
- Wide Operating Frequency :
10kHz to 800kHz

Pin Configuration



General Description

The AAT1107 series provides an integrated two-channel pulse-width-modulation (PWM) solution for the power supply of DC-DC system, this device offers the systems engineer the flexibility to tailor the power supply circuitry to a specific application. Each channel contains its own error amplifier, PWM comparator, dead-time control and output driver. The under-voltage protection, oscillator, short circuit protection and voltage reference circuit are common for the two channels.

The AAT1107 contains one step-up (boost) circuit (CH-2) and one inverting (buck_boost) circuit (CH-1). Dead-time control (DTC) can be set to provide 0% to 100% dead time by resistive divider network. Soft start can be implemented by paralleling the DTC resistor with a capacitor. Two dead time control inputs are assigned for Ch-1 and Ch-2 individually, and dead time control inputs can be used to control on / off operation.

The maximum output currents of LDO regulator can be enlarging by connect a N_MOS FET (or NPN bipolar) as a source follow stage at out3 pin.

*Spec is subject to change without notice in this document.



Pin Description

Pin #	Name	I/O	Description
1	CT	I	External timing capacitance
2	RT	I	External timing resistance
3	INV3	I	Negative input for LDO amplifier
4	INV1	I	Negative input for error amplifier 1
5	FB1	I	Output for error amplifier 1
6	DTC1	I	Output 1 dead time / soft start setting
7	OUT1	O	Output 1
8	GND		Ground
9	V _{DD}	I	Power supply
10	OUT2	O	Output 2
11	DTC2	I	Output 2 dead time / soft start setting
12	FB2	I	Output for error amplifier 2
13	INV2	I	Negative input for error amplifier 2
14	OUT3	I	LDO output
15	SCP	I	Timer latch setting
16	V _{ref}	O	Reference voltage (2.505V) output



Absolute Maximum Ratings

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Supply voltage	V_{DD}	7	V
Input voltage (IN-, DTC)	V_I	V_{DD}	V
Output voltage	V_O	$V_{DD}+0.3$	V
Output current	I_O	-120/+120	mA
Operating free-air temperature range	T_{ope}	-20 to 85	°C
Storage temperature range	T_{stg}	-65 to 150	°C
Power dissipation	P_d	500	mW

Recommended Operating Conditions

	Symbol	Min	Max	Unit
Supply voltage, V_{DD}	V_{DD}	4.0	6.5	V
Input voltage, INV1, INV2, INV3	V_{cm}	0.5	1.6	V
Output voltage	V_O	0	V_{DD}	V
OSC capacitor	C_T	100	15000	pF
OSC resistor (Note 1)	R_T	5.1	50	k
Oscillator frequency	f_{OSC}	10	800	kHz
Output current, Iout1, Iout2	I_{O12}		+50/-50	mA
Output current, Iout3	I_{O3}		+30	mA
Operating free-air temperature	T_{ope}	-20	85	°C



Electrical Characteristics, $V_{DD} = 5.0V$ (Unless Otherwise Specified) (See Note 1)

Oscillator

Parameter		Test Condition	Min	Typ	Max	Unit
Frequency	f_{OSC}	$C_T = 220pF, R_T = 10k$	320	400	480	KHz
Frequency change with V_{DD}	f_{dv}	$V_{DD} = 4.0V$ to $6.0V$, $T_A = 25^\circ C$ $C_T = 220pF, R_T = 10k$		1		%

Under-voltage Protection

Parameter		Test Condition	Min	Typ	Max	Unit
Upper threshold voltage	V_{UPH}	$T_A = 25^\circ C$	2.6	2.9	3.2	V
Lower threshold voltage	V_{UPL}	$T_A = 25^\circ C$	2.23	2.53	2.83	V
Hysteresis ($V_{UPH} - V_{UPL}$)	V_{HYS}	$T_A = 25^\circ C$		0.37		V

Short Circuit Protection Control

Parameter		Test Condition	Min	Typ	Max	Unit
Input threshold voltage	V_{r1}	Ch-2	2.1	2.4	2.65	V
Input threshold voltage	V_{r3}	Ch-1	0.95	1.05	1.15	V
Short-circuit detect threshold voltage	V_{r2}		1.48	1.64	1.8	V
SCP terminal source current	I_{SCP}		-1.5	-2.5	-3.5	μA
Standby Voltage	V_{STB}			50	100	mV
Latch Voltage	V_{LT}			30	100	mV

Note 1 : Typical values of all parameters are specified at $T_A = 25^\circ C$.



Electrical Characteristics, $V_{DD} = 5.0V$ (Unless Otherwise Specified) (See Note 1) (continued)
Reference Voltage

Parameter		Test Conditions	Min	Typ	Max	Unit
Internal reference Voltage	V_{refi}	$I_{REF} = -1mA, T_A = 25^\circ C$	1.220	1.233	1.246	V
Reference voltage	V_{REF}	$I_{REF} = -1mA, T_A = 25^\circ C$	2.430	2.505	2.580	
Input voltage regulation	V_{RI}	$I_{REF} = -1mA,$ $V_{DD} = 4.0V$ to $6.0V$		1	5	mV
Output regulation	V_{RO}	$I_{REF} = -0.1mA$ to $-1mA$		1		mV

EA (Error Amplifier)

Parameter		Test Condition	Min	Typ	Max	Unit
Input offset voltage	V_{IO}	Ch-1,2, $A_v=1$			6	mV
Input bias current	I_{IB}	Ch-1,2		± 15	± 100	nA
Input voltage range	V_{IR}	Ch-1,2	0.5		1.6	V
Open-loop voltage amplification	A_{VD}		70	85		dB
Output voltage swing	V_{OM+}		2.3	2.5		V
	V_{OM-}			0.7	0.9	
Output sink current	I_{OM+}	FB=1.25V	3	20		mA
Output source current	I_{OM-}	FB=1.25V	-45	-75		μA
Common-mode rejection ratio	CMRR		60	80		dB



Electrical Characteristics, $V_{DD} = 5.0V$ (Unless Otherwise Specified) (See Note 1) (continued)

Dead Time Control & PWM

Parameter		Test Condition	Min	Typ	Max	Unit
Input bias current	I_{BDT}	$V_{DTC} = 2V$		0.1	1	μA
Input threshold voltage (DTC1)	V_{1d0}	Duty = 0%, $f_{OSC} = 10kHz$	1.87	1.97	2.07	V
	V_{1d100}	Duty = 100%, $f_{OSC} = 10kHz$	1.38	1.48	1.58	
Input threshold voltage (DTC2)	V_{2d0}	Duty = 0%, $f_{OSC} = 10kHz$	1.38	1.48	1.58	V
	V_{2d100}	Duty = 100%, $f_{OSC} = 10kHz$	1.87	1.97	2.07	
Latch input voltage (DTC1)	V_{1DT}	$I_{DT} = 40\mu A$	2.28	2.48		V
Latch input voltage (DTC2)	V_{2DT}	$I_{DT} = 100\mu A$		0.1	0.3	V
Latch mode source current (DTC1)	I_{1DT}	DTC1=0V	-200	-560		μA
Latch mode source current (DTC2)	I_{2DT}	DTC2=2.0V	200	560		μA

Output Stage

Parameter		Test Condition	Min	Typ	Max	Unit
High-level output voltage	V_{OH}	$I_O = -50mA$	3.6	4.0		V
Low-level output voltage	V_{OL}	$I_O = +50mA$		0.8	1.2	V
Rise time	T_{rise}	$C_L = 1000pF$		100		nS
Fail time	T_{fail}	$C_L = 1000pF$		100		nS
Leakage current	I_{peak}	$V_o = 6.0V$			5	μA

LDO

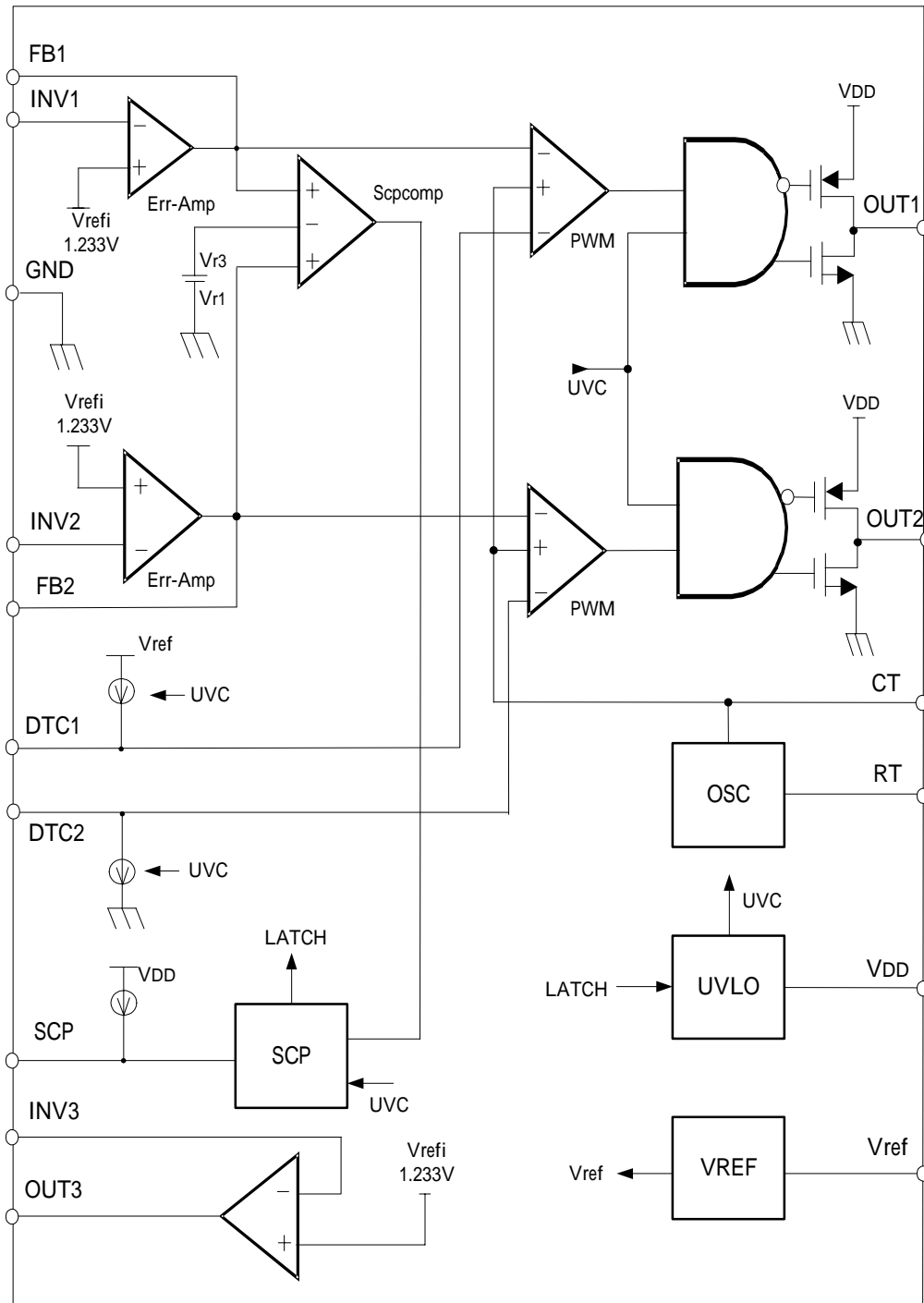
Parameter		Test Condition	Min	Typ	Max	Unit
Output voltage	V_{rd}	$V_{DD} = 5V, V_{out3} = 3.3V$	3.17	3.3	3.43	V
Line Regulation	LR_I	$V_{DD} = 4V \sim 6.5V,$ $I_{out3} = 10mA$		0.08	0.3	%
Load Regulation	LR_O	$I_{out3} = 1mA \sim 30mA$		0.1		%

Operating Current

Parameter		Test Condition	Min	Typ	Max	Unit
Supply current	I_{DD-OFF}	Output "OFF" state		1.8		mA
	I_{DD-ON}	$R_T = 10k$		2.0		mA



Function Block Diagram

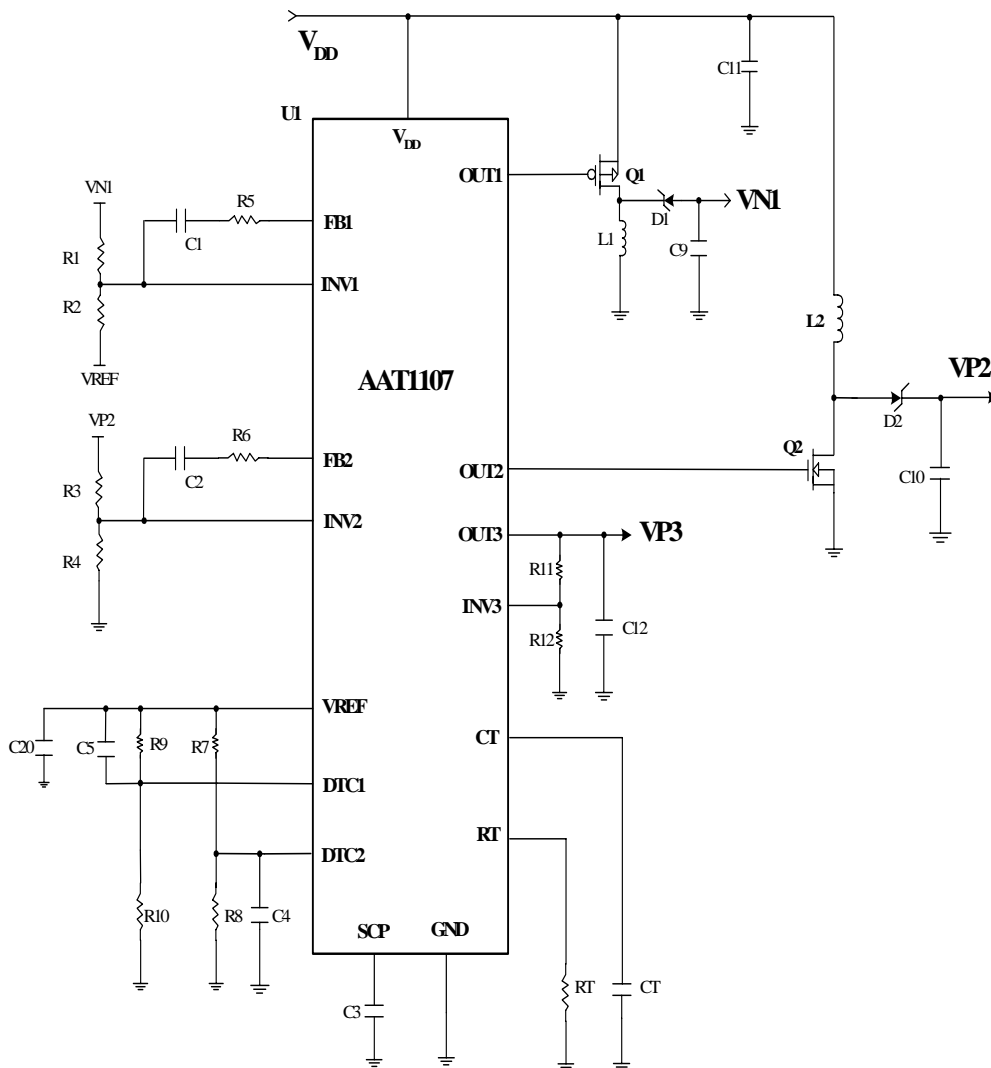


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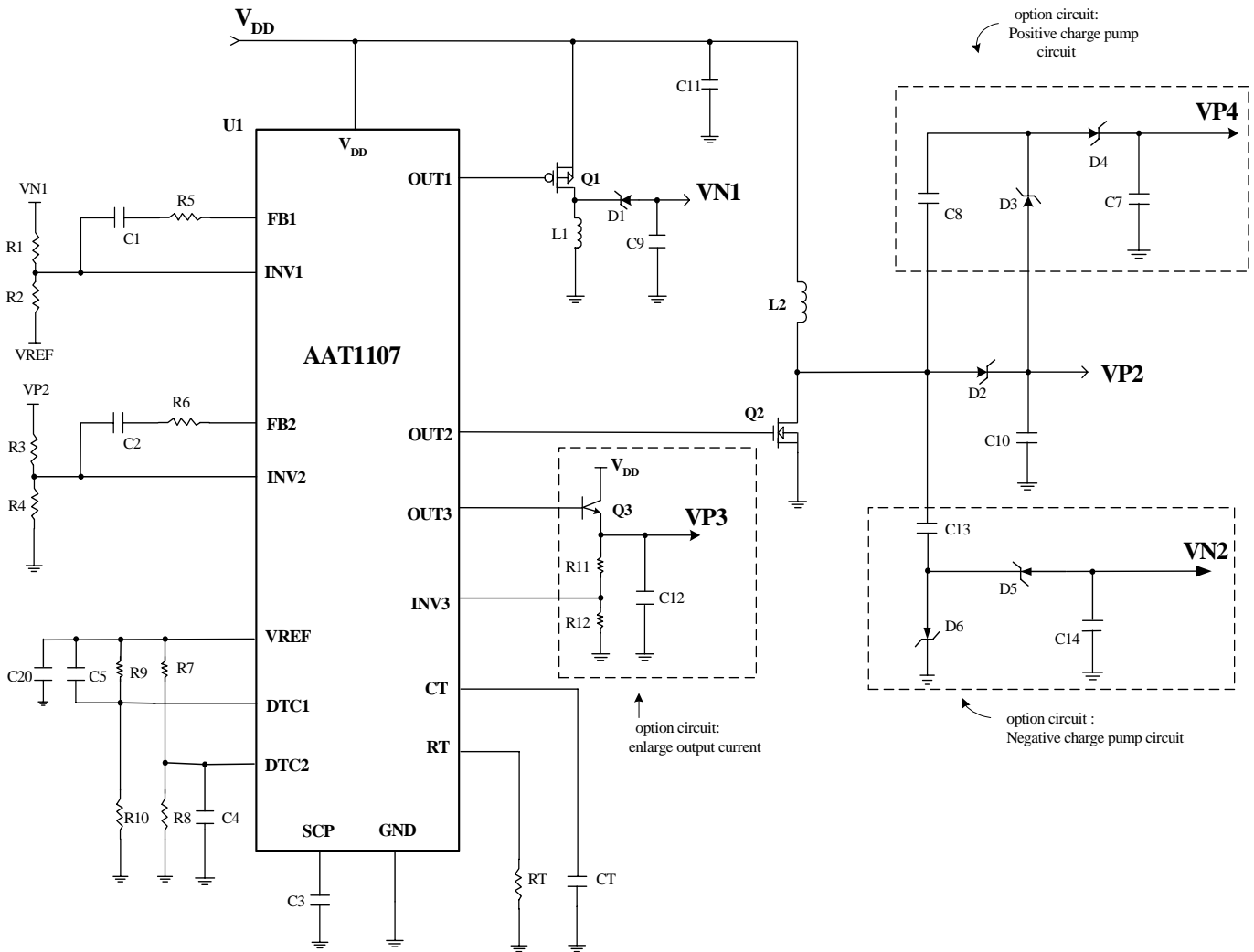


Application Circuit 1



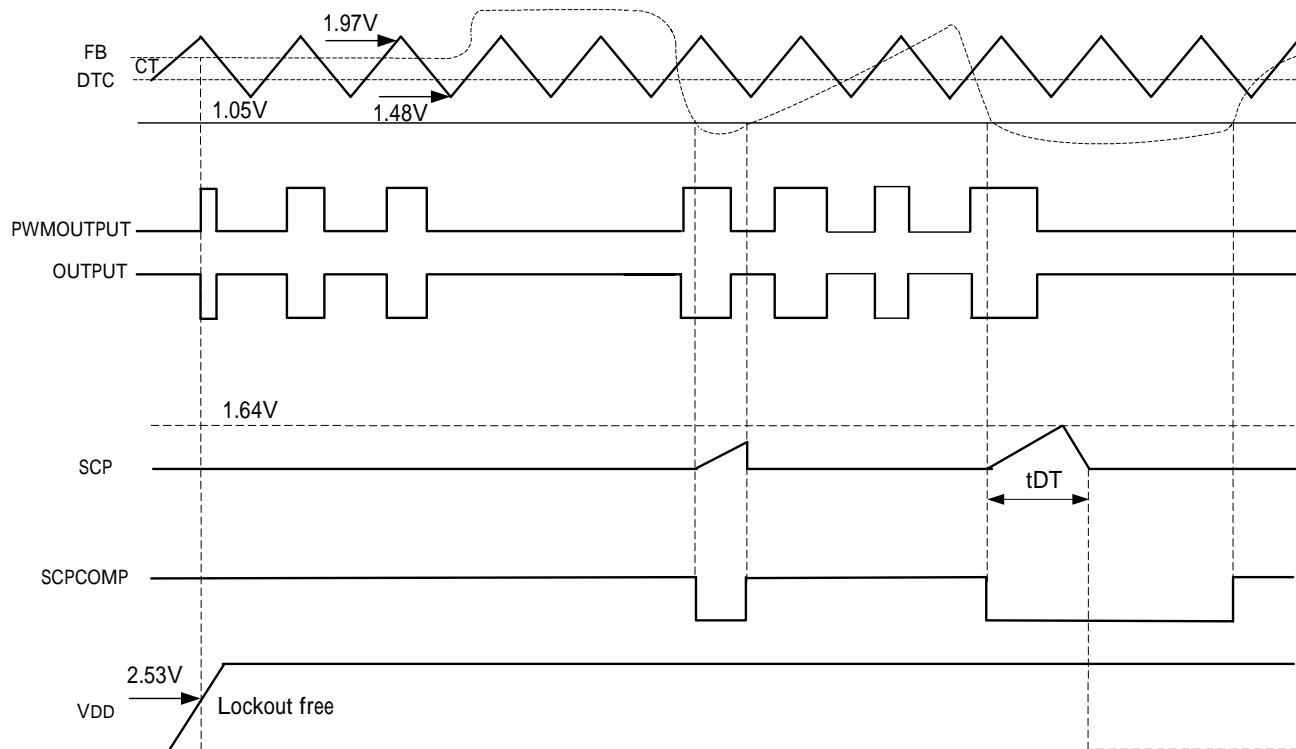


Application Circuit 2



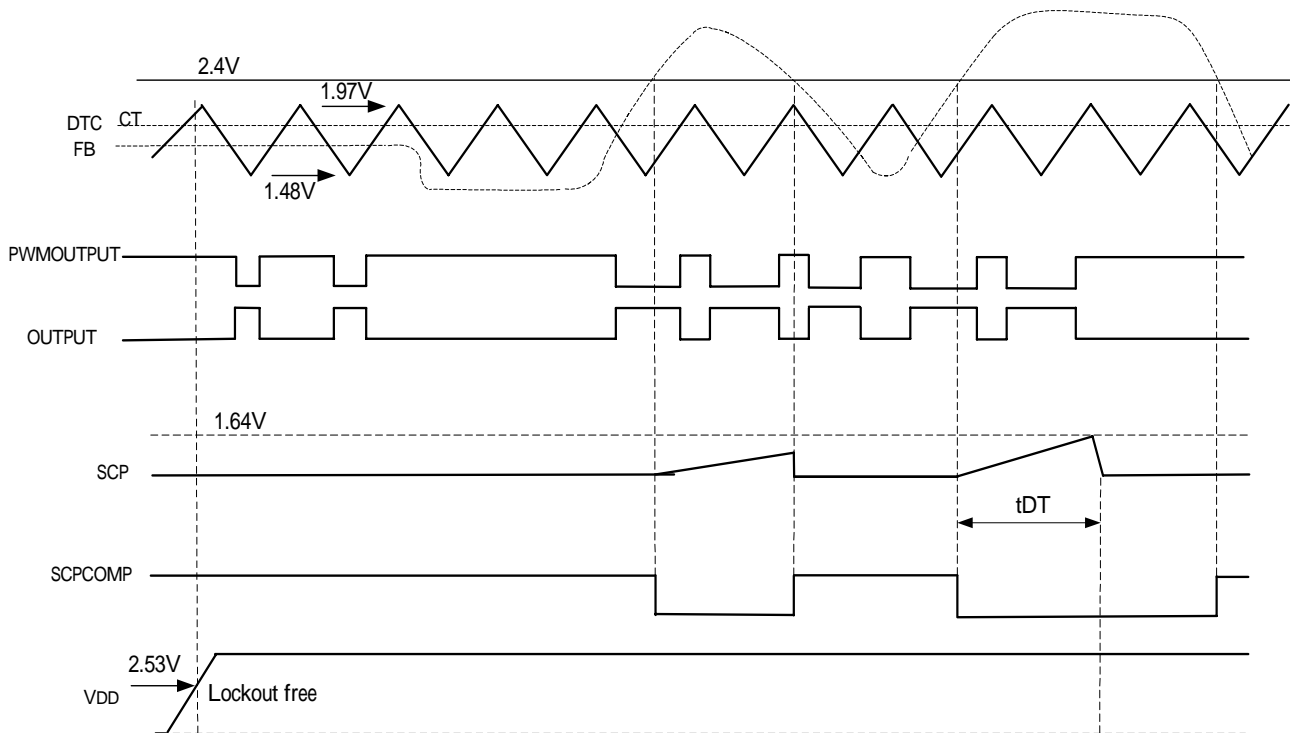


Buck-Boost (Inverting) Timing Chart (CH1)



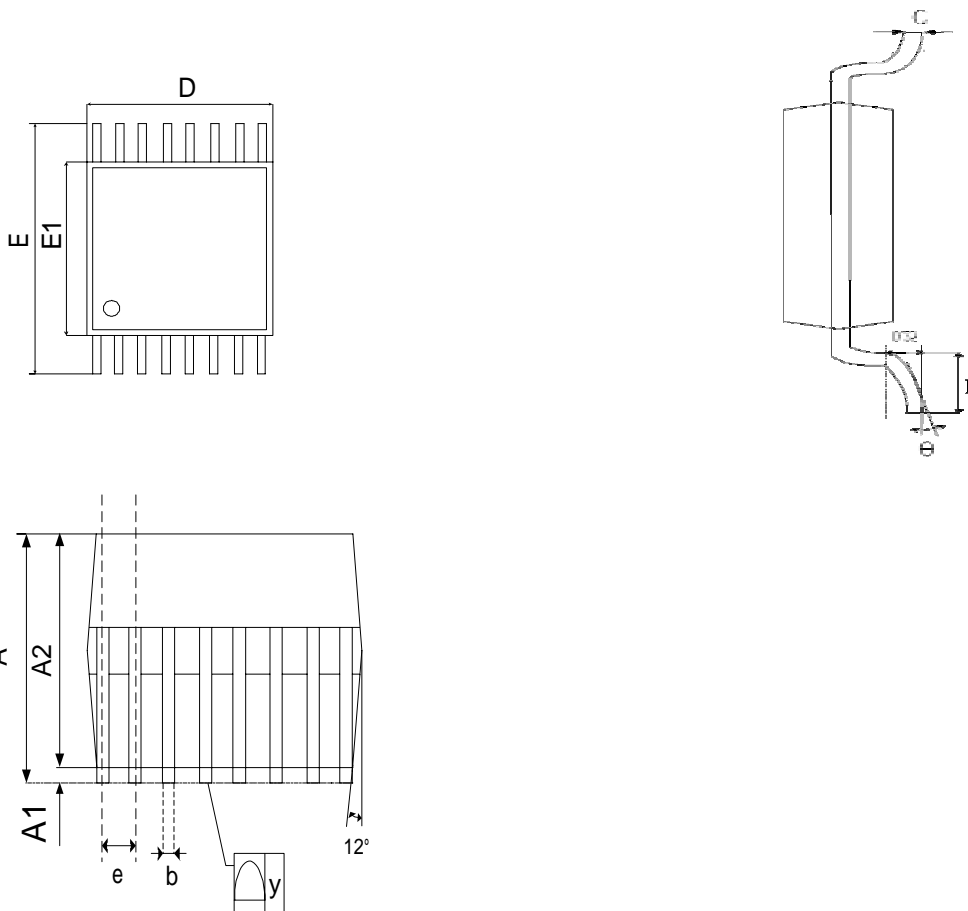


Boost (Step-up) Timing Chart (CH-2)





Package Dimension (Unit: Mil)



	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.10	1.20	0.041	0.043	0.047
A 1	0.05	0.10	0.15	0.002	0.004	0.006
A 2	—	1.00	1.05	—	0.039	0.041
b	0.20	0.25	0.28	0.008	0.010	0.011
C	—	0.127	—	—	0.005	—
D	4.90	5.075	5.10	0.193	0.1998	0.200
E	6.20	6.40	6.60	0.244	0.252	0.260
E 1	4.30	4.40	4.50	0.170	0.173	0.177
e	—	0.65	—	—	0.026	—
L	0.5	0.60	0.70	0.02	0.024	0.028
y	—	—	0.076	—	—	0.003
	0°	4°	8°	0°	4°	8°



NOTE:

1. Controlling dimension : mm
2. Dimension "D" does not include mold flash, the bar burrs and gate burrs.
Mold flash, the bar burrs and gate burrs shall not exceed 0.006"[0.15mm]
per end.
Dimension "E1" does not include interlead flash.
interlead flash shall not exceed 0.010"[0.25mm] per side.
3. Dimension "b" does not include dambar protrusion.
Allowable dambar protrusion shall be 0.003"[0.08mm] total in excess of
the "b" dimension at maximum material condition.
dambar cannot be located on the lower radius or the foot.
Minimum space between protrusion and an adjacent lead to be 0.0028"[0.07mm]
4. Tolerance: ± 0.010 "[0.25mm] unless otherwise specified.
5. Otherwise dimension follow acceptable spec.
